DATA FLOW SYNCHRONIZATION

BACKGROUND OF THE INVENTION

The present invention relates to synchronizing a data flow between devices.

For testing digital circuits, a device under test (DUT) typically receives a stimulus signal, and a response signal of the DUT on the stimulus signal is determined and e.g. compared with an expected response signal. Thus, errors can be determined e.g. when the determined response signals deviates from the expected response signal.

Such testing, however, requires that it is sufficiently clear when the actual response signal will appear, so that only such signals will be compared that actually correspond to each other. Otherwise, the test will most probably detect an error.

SUMMARY OF THE INVENTION

It is an object of the present invention to reduce errors occurring due to a mismatch between actual and expected response signals to be compared within a testing system. The object is solved by the independent claims. Preferred embodiments are shown by the dependent claims.

According to the invention, a testing unit for testing e.g. a digital circuit as device under test (DUT) comprises a signal generator for applying a stimulus signal to the DUT. A synchronizing unit is coupled between an output of the DUT and a receiving unit of the testing unit. The testing unit might further provide an analyzing unit for comparing the received response signal from the DUT with an expected response signal.

The response signal from the DUT is applied to the synchronizing unit using a DUT clock rate as provided by the DUT. The synchronizing unit buffers the response signal applied from the DUT or, in other words, provides a certain delay time to the response signal. The receiving unit reads out the buffered

response signal from the synchronizing unit, however, using a clock rate as provided by the testing unit for reading out. Thus, the delay time provided by the synchronizing unit depends on an initial delay time and the history of mismatch between DUT and testing unit characteristics or, in other words, the difference between the application of data to and the reading out from the synchronizing unit.

Hence, the invention allows balancing variations between the clock rates of the DUT and the testing unit. Such variations can be caused e.g. due to cumulative phase error in source synchronous clocks or due to variations of the phases of the different clocks. Further reasons can be that a DUT data protocol allows such variations because a data valid signal alarm is always provided.

For balancing such clock rates variations, synchronization circuits as disclosed e.g. in US-A-6,055,285, US-A-5,323,426,or US-A-5,867,672 can be applied acordingly.

In a preferred embodiment, the synchronizing unit comprises a structure with a plurality of registers. This structure might be a FIFO (first in first out) structure as well known in the art. A write pointer can be moved between the individual registers and defines which one of the pluralities of registers will receive a respective data word provided by the response signal from the DUT. Correspondingly, a read pointer can also be moved between the respective registers and defines which one of the registers the receiving unit can read out. While the write pointer will be clocked using the DUT clock for successively writing successive data words from the response signals to different registers, the read pointer will be clocked using the clock of the testing unit for successively reading out successive data words of the response signal buffered in the synchronizing unit.

Preferably, the synchronizing unit further comprises a latch controlled by the DUT clock, so that successive data words of the response signal will be latched with the DUT clock and thus successively written into successive registers.

In a further preferred embodiment, the initial delay time between a first (valid) write access from the DUT and a first (valid) read access by the receiving unit onto that written data word is provided dependent on the maximum expected variation between such write and read accesses. In the example of a synchronizing unit with a set of registers, the delay time can be determined by the number of registers between corresponding write and read accesses. Preferably, the initial delay time is set as half of the number of registers. In an example of a structure with eight registers, the initial delay time is preferably set to four registers. It is clear that the maximum delay time of the synchronizing unit has to be adjusted to cover all expected variations as e.g. known from prior tests or as specified for the DUT.

In another preferred embodiment, an initialization process is provided to initialize a first valid write access and/or a first valid read access. This can be accomplished e.g. by utilizing known reference signals having a known timing characteristics. So far there are two basic types:

1. Somewhere in the beginning of the DUT response data stream, the time of the response is known in data stream with an accuracy better than the duration of one clock of the testing unit. In this case the testing unit can determine the start position and time of the read and the write pointer.

2. The DUT provides a signal that indicates where to start. In this case the DUT will control the start of the write pointer and the testing unit will determine the start of the read pointer. For this the accuracy of the knowledge about the response time can be several clocks, but certainly not more than registers are there. In other words the amount of registers has to be more than the uncertainty range of the DUT response.

The invention can be partly or entirely embodied or supported by one or more suitable software programs, which can be stored on or otherwise provided by any kind of data carrier, and which might be executed in or by any suitable data

processing unit. In particular, software tools can be used in conjunction with user test programs, or as system software to enable the synchronization feature.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and many of the attendant advantages of the present invention will be readily appreciated and become better understood by reference to the following detailed description when considering in connection with the accompanied drawing.

Figure 1 shows a preferred test structure for a testing unit 10 according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In Fig. 1, a signal generator 20 provides a stimulus signal to a device under test DUT 30. A signal response of the DUT 30 on the stimulus signal is provided via a synchronizing unit 40 to a receiving unit 50. An analyzing unit 60 compares the response signal as received by the receiving unit 50 with an expected response signal for determining whether the DUT 30 behaves in the expected way or whether errors occur. Dependent on the application, the analyzing unit 60 might control the signal generator 20 and/or the stimulus signal as provided by the signal generator 20 or receive this stimulus signal.

It is clear that while the testing unit 10 comprises the signal generator 20, the synchronizing unit 40, the receiving unit 50, and the analyzing unit 60, the DUT 30 is not part thereof.

The synchronizing unit 40 further receives a clock signal DUT-CLK from the DUT 30 and a clock signal CLK of the testing unit 10. The clock signal DUT-CLK might be the internal clock signal of the DUT 30 or derived therefrom. Accordingly, the clock signal CLK might be the internal clock signal of the testing unit 10 or derived therefrom.

The synchronizing unit 40 provides synchronization between the provision of the response signal from the DUT 30 and the receiving of the corresponding response signal by the receiving unit 50. Thus, it can be ensured that a certain event within the response signal from the DUT 30 can be unambiguously assigned to a corresponding event in the expected response signal, so that temporal mismatches between the actual and the expected response signal can be avoided, and that only corresponding events within the actual and expected response signal will be compared by that analyzing unit 60.

In the preferred embodiment of Figure 1, the synchronizing unit 40 comprises a delay unit 70 having a structure with a plurality of individual registers 70A, 70B, ... In the specific example of Figure 1, the delay unit 70 comprises eight registers 70A – 70H. A write unit 80 receives the response signal from the DUT 30 and successively writes successive data words of the response signal into successive registers of the delay unit 70. Accordingly, a read unit 90 successively reads out successive data words of the response signal as stored in the delay unit 70 and provides those data words to the receiving unit 50.

Not shown in Figure 1, the write unit 80 might comprise a latching unit controlled by the clock DUT-CLK for covering the timing variations less than the duration time of one clock.

Since the number of registers in the delay unit 70 is naturally limited, the delay unit 70 in conjunction with the write unit 80 and the read unit 90 preferably provides a FIFO structure, wherein the individual registers of the delay unit 70 are repeatedly written and read out e.g. in a circular manner as indicated in Figure 1. For that purpose, a write pointer 100 of the write unit 80 is repeatedly moved between the registers 70A – 70H, so that the registers of the delay unit 70 will be rewritten with each writing cycle. Accordingly, a read pointer 110 is moved repeatedly between the registers 70A-70H.

It is clear that the write accesses as provided by the write pointer 100 have to stay within limits in relation to the read accesses as provided by the read pointer 110, so that it is, on one hand, avoided that the write unit 80 will

overwrite data in the delay unit 70 before it has been read out by the read unit 90, and, on the other hand, that it is avoided that the read unit 90 reads faster than the write unit 80 can write, so that the read unit 90 will virtually "overtake" the write unit 80. For that purpose, the clock rates DUT-CLK and CLK should be synchronized to a certain extend. Further, the number of registers 70i, with i = A, B, ..., of the delay unit 70, should be adapted to the maximum expected valid difference between corresponding read and write accesses.

In the example of Figure 1 the rates of the clocks DUT-CLK and CLK are set to be equal, so that the synchronizing unit 40 only needs to balance phase mismatches between the clocks DUT-CLK and CLK. Further in the specific example of Figure 1, an initial delay time between corresponding read and write accesses will be set to half of the number of registers in the delay unit 70. In the example of Figure 1, the initial delay time will be set to four registers. That means that while the write unit 80 e.g. writes to register 70F, the read unit 90 initially reads out register 70B.

As shown in Figure 1, the write unit 80 will be clocked with the clock DUT-CLK as provided from the DUT 30, so that the write pointer 100 will be moved to the successive register with each successive clock cycle of the clock signal DUT-CLK. The read pointer 100, however, will be moved to a successive register with each successive cycle of the clock signal CLK as of the testing unit 10. That means that once the initial delay time has been set, deviations between the clocks DUT-CLK and CLK will also lead to deviations between corresponding read and write accesses for the same data word. In an example with an initial delay time of "four registers" in an eight registers structure, the number of registers between corresponding read and write accesses might decreased to 3, 2 or only 1 register or increase to 5, 6 or maximum 7 registers. However, as long as the minimum and maximum differences between corresponding read and write accesses are not exceeded, such deviations will be balanced by the synchronizing unit 40, so that the data integrity of the actual response signal with respect to the expected response signal can be

preserved.

For initializing the synchronizing unit 40, both pointers 100 and 110 are preferably set in a reset mode e.g. pointing to register 70A, while the clocks DUT-CLK and CLK are turned off (or disabled) within the synchronizing unit 40. Thus, all coming data is ignored during the reset mode. With a valid signal "write start" it is indicated that the response signals from the DUT are valid now. With the write start signal, the clock DUT-CLK for the write unit 80 will be opened (or enabled) again, and data will be written successively with each cycle of the clock DUT-CLK into the registers 70A – 70H repeatedly. With a valid signal "read start" it is indicated that the read unit 90 shall now be enabled to read out data from the delay unit 70. The clock signal CLK of the testing unit 10 will be opened again for the read unit 90, and data will be read out from the registers 70A-70H successively with each cycle of the clock CLK. The temporal difference between the appearance of the valid signals 'read start' and 'write start' represents the initial delay time.

Further possible variations of implementation for the initializations are:

1. The amount of registers is increased to compensate some propagation delay in the system as well. After reset the read and write pointers are clocked together with DUT-CLK, but the read pointer is always running some registers behind. With the write start event the read pointer will halt. With the read start event the read pointer will be clocked by the clock of the testing unit.

2. With no initial difference, the previous implementation variant would be compatible with very first described.